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Phoenix and Cluster II
RAPID

Customizing the IES Software

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Contents

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1 Generation of IES look-up tables (LUT)

The IES generates 8-bit energy results. The 256 possible values are sorted into 16 energy bins, which are available for every IES look direction (ID).

E-ADC Channel range Range: 0…255	Bin number Range: 0…15
0	0
1…(P-2S-1)	1
(P-2S)…(P-S-1)	2
(P-S)…(P-1)	3
P…(P+S-1)	4
(P+S)…(P+2S-1)	5
(P+2S)…(P+B1-1)	6
(P+B1)…(P+B2-1)	7
(P+B2)…(P+B3-1)	8
(P+B3)…(P+B4-1)	9
(P+B4)…(P+B5-1)	10
(P+B5)…(P+B6-1)	11
(P+B6)…(P+B7-1)	12
(P+B7)…(P+B8-1)	13
(P+B8)…254	14
255	15

Table 1-1 Principle of ADC channel assignment to bin numbers

Generation of the EPP look-up tables is a sequence of up to four steps. With each step the data format of the LUT changes from a parameterized to a fully expanded description. Thus there are five different data formats that are described in section 1.2. It is possible to change the contents of the data in three of the five formats.

1.1 Data flow and default commands

The building of an LUT is done in four steps:

1. A two-parameter LUT description is copied from EPROM into RAM. This copy contains 4 LUT descriptions for a given temperature and the 4 different integration times.

2. The two-parameter description in conjunction with the 8 bin boundary offsets B1-B8 is used to calculate a sixteen-parameter description of the LUTs. Also here the four tables for each integration time exist in parallel for a given temperature.

3. One selected sixteen-parameter description is used to build the complete, expanded LUT for a given temperature, one integration time and for all IES look directions (ID). This table is of large size (16*256=4096 bytes) and covers also the invalid ID numbers.

4. The expanded LUT is copied from RAM into the dedicated EPP H/W memory. This is done for both memory pages of the EPP.

After power-up of the instrument the above four steps are performed automatically, thus providing the standard IES LUT (20°C, 2µs). Autoswitching is enabled (compare Section 2). No additional command is necessary to achieve this status.

Selection of the one integration time is done via the RAPID command ZERELUTS. The parameters for this command are 0,1,2 and 3 (2, 5, 15, 50 µs) with autoswitching enabled, and 40h, 41h, 42h and 43h (2, 5, 15, 50 µs) with autoswitching disabled.

1.2 Data format and location

The four steps of a LUT generation are transitions between 5 different forms of LUT representations. In the following subsections these LUT descriptions are explained.

1.2.1 Two-parameter default LUT description

The instrument's EPROM contains just 1 default set of LUT descriptions.

		2µs	5µs	15µs	50µs
ID1	**P**	22	22	18	16
	S	3	4	6	7
ID2	**P**	27	27	24	22
	S	3	4	6	7
ID3	**P**	22	22	19	17
	S	3	4	6	7
ID4	**P**	21	21	18	17
	S	3	4	6	7
ID5	**P**	29	29	26	25
	S	3	4	6	7
ID6	**P**	22	21	18	16
	S	3	4	6	7
ID7	**P**	18	17	14	11
	S	3	4	6	7
ID8	**P**	13	13	10	8
	S	3	4	6	7
ID9	**P**	16	16	12	10
	S	3	4	6	7

Table 1-2 Two-parameter default LUT description in EPROM

The default set is based on measurements that have been made at 20°C temperature with the F1 (phoenix) IES in december 1996. Thus the values for 5-50 µs were measured with the old integration times of 10-100 µs and may need to be corrected.

1.2.2 Two-parameter LUT description

With instrument power-on a copy of the default set in Table 1-2 is transferred from EPROM to RAM. Another way of copying this data set is to use the RAPID command *ZERELUTS 80h*.

Other parameters than 80h are not useful, because the additional default sets are not filled with meaningful data. This part of the RAM can be stored into non-volatile memory (NVRAM).

```
(OFFS +) 25172-79    00   16   03   1B   03   16   03   15
(OFFS +) 2517A-81    03   1D   03   16   03   12   03   0D
(OFFS +) 25182-89    03   10   03   80   16   04   1B   04
(OFFS +) 2518A-91    16   04   15   04   1D   04   15   04
(OFFS +) 25192-99    11   04   0D   04   10   04   40   12
(OFFS +) 2519A-A1    06   18   06   13   06   12   06   1A
(OFFS +) 251A2-A9    06   12   06   0E   06   0A   06   0C
(OFFS +) 251AA-B1    06   C0   10   07   16   07   11   07
(OFFS +) 251B2-B9    11   07   19   07   10   07   0B   07
(OFFS +) 251BA-BD    08   07   0A   07
```

Table 1-3 Memory dump of two-parameter LUT description in RAM (default) [i]

Selected parameters or even the whole data set can be edited. The changes can be stored in NVRAM by issuing the RAPID command *ZERCFGSS 0*. Reloading of the data set at a later time can be done through the command *ZERCFGSS 1*.

The two-parameter description is built from four adjacent tables, each consisting of 1 integration time command byte + 2 parameter bytes (P,S) for each ID 1to 9, resulting in a table size of 4*(1+9*2)=76 bytes.

Boundary offsets

The default values for the eight boundary offsets B1-B8 are:

B1	B2	B3	B4	B5	B6	B7	B8
21	29	41	56	78	109	151	210

Table 1-4 Default values for boundary offsets B1-B8

With power-on B1-B8 are copied into RAM. This part of the RAM can be stored into non-volatile memory (NVRAM).

```
(OFFS +) 24EF6-FD    15   1D   29   38   4E   6D   97   D2
```

Table 1-5 Memory dumps of boundary offsets B1-B8 in RAM [i]

Selected parameters or even the whole data set can be edited. The changes can be stored in NVRAM by issuing the RAPID command *ZERCFGSS 0*. Reloading of the data set at a later time can be done through the command *ZERCFGSS 1*.

1.2.3 Sixteen-parameter LUT description

The 2-parameter description in conjunction with the Boundary offsets (both described in Section 1.2.2) is taken to calculate a 16-parameter description of a single LUT. The 16 parameters represent the upper boundaries (in ADC channels) for a given bin.

(OFFS +) 24F2E-35	00	00	0F	12	15	18	1B	2A
(OFFS +) 24F36-3D	32	3E	4D	63	82	AC	E7	FE
(OFFS +) 24F3E-45	FF	00	14	17	1A	1D	20	2F
(OFFS +) 24F46-4D	37	43	52	68	87	B1	EC	FE
(OFFS +) 24F4E-55	FF	00	0F	12	15	18	1B	2A
(OFFS +) 24F56-5D	32	3E	4D	63	82	AC	E7	FE
(OFFS +) 24F5E-65	FF	00	0E	11	14	17	1A	29
(OFFS +) 24F66-6D	31	3D	4C	62	81	AB	E6	FE
(OFFS +) 24F6E-75	FF	00	16	19	1C	1F	22	31
(OFFS +) 24F76-7D	39	45	54	6A	89	B3	EE	FE
(OFFS +) 24F7E-85	FF	00	0F	12	15	18	1B	2A
(OFFS +) 24F86-8D	32	3E	4D	63	82	AC	E7	FE
(OFFS +) 24F8E-95	FF	00	0B	0E	11	14	17	26
(OFFS +) 24F96-9D	2E	3A	49	5F	7E	A8	E3	FE
(OFFS +) 24F9E-A5	FF	00	06	09	0C	0F	12	21
(OFFS +) 24FA6-AD	29	35	44	5A	79	A3	DE	FE
(OFFS +) 24FAE-B5	FF	00	09	0C	0F	12	15	24
(OFFS +) 24FB6-BD	2C	38	47	5D	7C	A6	E1	FE
(OFFS +) 24FBE	FF							

Table 1-6 Memory dump of 16-parameter LUT description (2µs) [i]

(OFFS +) 24FBF-C6	80	00	0D	11	15	19	1D	2A
(OFFS +) 24FC7-CE	32	3E	4D	63	82	AC	E7	FE
(OFFS +) 24FCF-D6	FF	00	12	16	1A	1E	22	2F
(OFFS +) 24FD7-DE	37	43	52	68	87	B1	EC	FE
(OFFS +) 24FDF-E6	FF	00	0D	11	15	19	1D	2A
(OFFS +) 24FE7-EE	32	3E	4D	63	82	AC	E7	FE
(OFFS +) 24FEF-F6	FF	00	0C	10	14	18	1C	29
(OFFS +) 24FF7-FE	31	3D	4C	62	81	AB	E6	FE
(OFFS +) 24FFF-06	FF	00	14	18	1C	20	24	31
(OFFS +) 25007-0E	39	45	54	6A	89	B3	EE	FE
(OFFS +) 2500F-16	FF	00	0C	10	14	18	1C	29
(OFFS +) 25017-1E	31	3D	4C	62	81	AB	E6	FE
(OFFS +) 2501F-26	FF	00	08	0C	10	14	18	25
(OFFS +) 25027-2E	2D	39	48	5E	7D	A7	E2	FE
(OFFS +) 2502F-36	FF	00	04	08	0C	10	14	21
(OFFS +) 25037-3E	29	35	44	5A	79	A3	DE	FE
(OFFS +) 2503F-46	FF	00	07	0B	0F	13	17	24
(OFFS +) 25047-4E	2C	38	47	5D	7C	A6	E1	FE
(OFFS +) 2504F	FF							

Table 1-7 Memory dump of 16-parameter LUT description (5µs) [i]

(OFFS +) 25050-57	40	00	05	0B	11	17	1D	26
(OFFS +) 25058-5F	2E	3A	49	5F	7E	A8	E3	FE
(OFFS +) 25060-67	FF	00	0B	11	17	1D	23	2C
(OFFS +) 25068-6F	34	40	4F	65	84	AE	E9	FE
(OFFS +) 25070-77	FF	00	06	0C	12	18	1E	27
(OFFS +) 25078-7F	2F	3B	4A	60	7F	A9	E4	FE
(OFFS +) 25080-87	FF	00	05	0B	11	17	1D	26
(OFFS +) 25088-8F	2E	3A	49	5F	7E	A8	E3	FE
(OFFS +) 25090-97	FF	00	0D	13	19	1F	25	2E
(OFFS +) 25098-9F	36	42	51	67	86	B0	EB	FE
(OFFS +) 250A0-A7	FF	00	05	0B	11	17	1D	26
(OFFS +) 250A8-AF	2E	3A	49	5F	7E	A8	E3	FE
(OFFS +) 250B0-B7	FF	00	01	07	0D	13	19	22
(OFFS +) 250B8-BF	2A	36	45	5B	7A	A4	DF	FE
(OFFS +) 250C0-C7	FF	00	01	03	09	0F	15	1E
(OFFS +) 250C8-CF	26	32	41	57	76	A0	DB	FE
(OFFS +) 250D0-D7	FF	00	01	05	0B	11	17	20
(OFFS +) 250D8-DF	28	34	43	59	78	A2	DD	FE
(OFFS +) 250E0	FF							

Table 1-8 Memory dump of 16-parameter LUT description (15µs) [i]

(OFFS +) 250E1-E8	C0	00	01	08	0F	16	1D	24
(OFFS +) 250E9-F0	2C	38	47	5D	7C	A6	E1	FE
(OFFS +) 250F1-F8	FF	00	07	0E	15	1C	23	2A
(OFFS +) 250F9-00	32	3E	4D	63	82	AC	E7	FE
(OFFS +) 25101-08	FF	00	02	09	10	17	1E	25
(OFFS +) 25109-10	2D	39	48	5E	7D	A7	E2	FE
(OFFS +) 25111-18	FF	00	02	09	10	17	1E	25
(OFFS +) 25119-20	2D	39	48	5E	7D	A7	E2	FE
(OFFS +) 25121-28	FF	00	0A	11	18	1F	26	2D
(OFFS +) 25129-30	35	41	50	66	85	AF	EA	FE
(OFFS +) 25131-38	FF	00	01	08	0F	16	1D	24
(OFFS +) 25139-40	2C	38	47	5D	7C	A6	E1	FE
(OFFS +) 25141-48	FF	00	01	03	0A	11	18	1F
(OFFS +) 25149-50	27	33	42	58	77	A1	DC	FE
(OFFS +) 25151-58	FF	00	01	02	07	0E	15	1C
(OFFS +) 25159-60	24	30	3F	55	74	9E	D9	FE
(OFFS +) 25161-68	FF	00	01	02	09	10	17	1E
(OFFS +) 25169-70	26	32	41	57	76	A0	DB	FE
(OFFS +) 25171	FF							

Table 1-7 Memory dump of 16-parameter LUT description (50µs) [i]

Each of the tables in this section consists of 1 IES integration time command byte followed by 9 ID descriptions with 16 upper bin boundaries, each.

Selected parameters or even the whole data set can be edited. The changes can be stored in NVRAM by issuing the RAPID command *ZERCFGSS 0*. Reloading of the data set at a later time can be done through the command *ZERCFGSS 1*.

1.2.4 Expanded LUT in RAM

Issuing the RAPID command *ZERELUTS n* (*n*:0,1,2,3) initiates the selection of the integration time and the above calculation of a sixteen-parameter description. With this information an integration time specific LUT can be expanded into RAM. Prior to loading this LUT into the EPP memory it is possible to edit this table. The resulting LUT however will vanish with every instrument power-off, so editing at this stage has to be repeated after every power-on sequence of the instrument. In the following an excerpt (ID1 and ID2) of the 2 µs default table is shown. The lower four bits of each byte represent the bin number, wheras the upper four bits stand for the ID number. The complete LUT consists of 16 ID sections (ID 0 and 10 to 15 filled with FFh) each with 256 LUT entries, one for each ADC channel.

The LUT start address for any ID 1 to 9 can be calculated from:

$$Startaddress = 13F44h + 256 \cdot (ID - 1)$$

13F44-4B	10	11	11	11	11	11	11	11
13F4C-53	11	11	11	11	11	11	11	11
13F54-5B	12	12	12	13	13	13	14	14
13F5C-63	14	15	15	15	16	16	16	16
13F64-6B	16	16	16	16	16	16	16	16
13F6C-73	16	16	16	17	17	17	17	17
13F74-7B	17	17	17	18	18	18	18	18
13F7C-83	18	18	18	18	18	18	18	19
13F84-8B	19	19	19	19	19	19	19	19
13F8C-93	19	19	19	19	19	19	1A	1A
13F94-9B	1A	1A	1A	1A	1A	1A	1A	1A
13F9C-A3	1A	1A	1A	1A	1A	1A	1A	1A
13FA4-AB	1A	1A	1A	1A	1B	1B	1B	1B
13FAC-B3	1B	1B	1B	1B	1B	1B	1B	1B
13FB4-BB	1B	1B	1B	1B	1B	1B	1B	1B
13FBC-C3	1B	1B	1B	1B	1B	1B	1B	1B
13FC4-CB	1B	1B	1B	1C	1C	1C	1C	1C
13FCC-D3	1C	1C	1C	1C	1C	1C	1C	1C
13FD4-DB	1C	1C	1C	1C	1C	1C	1C	1C
13FDC-E3	1C	1C	1C	1C	1C	1C	1C	1C
13FE4-EB	1C	1C	1C	1C	1C	1C	1C	1C
13FEC-F3	1C	1C	1C	1C	1C	1D	1D	1D
13FF4-FB	1D	1D	1D	1D	1D	1D	1D	1D
13FFC-03	1D	1D	1D	1D	1D	1D	1D	1D
14004-0B	1D	1D	1D	1D	1D	1D	1D	1D
1400C-13	1D	1D	1D	1D	1D	1D	1D	1D
14014-1B	1D	1D	1D	1D	1D	1D	1D	1D
1401C-23	1D	1D	1D	1D	1D	1D	1D	1D
14024-2B	1D	1D	1D	1D	1D	1D	1D	1D
1402C-33	1E	1E	1E	1E	1E	1E	1E	1E
14034-3B	1E	1E	1E	1E	1E	1E	1E	1E
1403C-43	1E	1E	1E	1E	1E	1E	1E	1F
14044-4B	20	21	21	21	21	21	21	21
1404C-53	21	21	21	21	21	21	21	21
14054-5B	21	21	21	21	21	22	22	22
1405C-63	23	23	23	24	24	24	25	25
14064-6B	25	26	26	26	26	26	26	26
1406C-73	26	26	26	26	26	26	26	26
14074-7B	27	27	27	27	27	27	27	27
1407C-83	28	28	28	28	28	28	28	28
14084-8B	28	28	28	28	29	29	29	29
1408C-93	29	29	29	29	29	29	29	29
14094-9B	29	29	29	2A	2A	2A	2A	2A
1409C-A3	2A	2A	2A	2A	2A	2A	2A	2A
140A4-AB	2A	2A	2A	2A	2A	2A	2A	2A
140AC-B3	2A	2B	2B	2B	2B	2B	2B	2B
140B4-BB	2B	2B	2B	2B	2B	2B	2B	2B
140BC-C3	2B	2B	2B	2B	2B	2B	2B	2B
140C4-CB	2B	2B	2B	2B	2B	2B	2B	2B
140CC-D3	2C	2C	2C	2C	2C	2C	2C	2C
140D4-DB	2C	2C	2C	2C	2C	2C	2C	2C
140DC-E3	2C	2C	2C	2C	2C	2C	2C	2C
140E4-EB	2C	2C	2C	2C	2C	2C	2C	2C
140EC-F3	2C	2C	2C	2C	2C	2C	2C	2C
140F4-FB	2C	2C	2D	2D	2D	2D	2D	2D
140FC-03	2D	2D	2D	2D	2D	2D	2D	2D
14104-0B	2D	2D	2D	2D	2D	2D	2D	2D
1410C-13	2D	2D	2D	2D	2D	2D	2D	2D
14114-1B	2D	2D	2D	2D	2D	2D	2D	2D
1411C-23	2D	2D	2D	2D	2D	2D	2D	2D
14124-2B	2D	2D	2D	2D	2D	2D	2D	2D
1412C-33	2D	2D	2D	2D	2D	2E	2E	2E
14134-3B	2E	2E	2E	2E	2E	2E	2E	2E
1413C-43	2E	2E	2E	2E	2E	2E	2E	2F

Table 1-8 Expanded LUT in RAM (example: ID1 and ID2 of 2µs)

1.2.5 Expanded LUT in EPP memory

A copy of the expanded LUT is transferred from RAM to each of the two EPP memory pages that are used as switching buffers. Editing at this stage is not recommended. The data format is the same as described in Section 1.2.4.

1.3 Customizing the LUTs

1.3.1 Uploading of description changes

Changes of the LUT description are easily possible for all RAM based tables. Changes in EPROM are not possible (no EEPROM used) and changes in the EPP memory are not recommended.

Changes in the RAM based tables can be made to complete descriptions or selected items. The upload sequence contains the start of the physical memory address range and thus is unique for every change. The address ranges involved are already indentified in the tables in Section 1.2.

1.3.2 Incorporating the LUT description changes

After uploading the new parameters the changes may have to be incorporated into the current LUT. The following Table 1-9 shows how to proceed for changes in the different tables.

Changes in …	Incorporate by sending …	Commands after power cycle
Two-parameter LUT description (see Section 1.2.2)	ZERCFGSS 0 ZERELUTS [0,1,2,3,40h,41h,42h,43h][1]	ZERCFGSS 1
Boundary offsets (see Section 1.2.2)	ZERCFGSS 0 ZERELUTS [0,1,2,3,40h,41h,42h,43h][1]	ZERCFGSS 1
Sixteen-parameter LUT description (see Section 0)	ZERCFGSS 0 BERJOBS ...[2] (2µs)[3] BERJOBS ...[4] (5µs)[3] BERJOBS ...[5] (15µs)[3] BERJOBS ...[6] (50µs)[3]	ZERCFGSS 1 BERJOBS ...[2] (2µs)[3] BERJOBS ...[4] (5µs)[3] BERJOBS ...[5] (15µs)[3] BERJOBS ...[6] (50µs)[3]
Complete expanded LUT (see Section 1.2.4)	ZERELUTS [40h,41h,42h,43h] [7] BERJOBS ...[8]	Repeat upload of changes ZERELUTS [40h,41h,42h,43h][7] BERJOBS ...[8]

Table 1-9 Command sequences for incorporating LUT description changes

[1] Send this command with any adequate parameter
[2] For RAPID F1 (phoenix) use the parameters ‘38h 59h 85h A1h’, for RAPID F6-F8 use ‘39h 22h 85h 9Ah’
[3] Command is only neccessary, if the description changes are in the currently used integration time.
[4] For RAPID F1 (phoenix) use the parameters ‘38h 65h 85h D0h’, for RAPID F6-F8 use ‘39h 2Eh 85h 60h’
[5] For RAPID F1 (phoenix) use the parameters ‘38h 71h 85h FFh’, for RAPID F6-F8 use ‘39h 3Ah 85h 4Fh’
[6] For RAPID F1 (phoenix) use the parameters ‘38h 7Dh 85h 05h’, for RAPID F6-F8 use ‘39h 46h 85h FBh’
[7] Changes in the expanded LUT may be unrecoverably overwritten, if autoswitching mode is enabled.
[8] For RAPID F1 (phoenix) use the parameters ‘3Ah 7Eh 85h 45h’, for RAPID F6-F8 use ‘36h 47h 85h c1h’

2 IES autoswitching

The IES autoswitching automatically adapts the IES integration time and LUT selection to the measured electron flux. In the case of high flux the integration time shall be shortenend to avoid pedestal (energy = 0 keV) movement, in the case of low flux the integration time will be widened to achieve statistically significant count rates. The autoswitching can be disabled by using the RAPID command ZERELUTS with bit 6 set to 1. By default autoswitching is enabled.

2.1 Algorithm

In the current default configuration the algorithm is as follows:

For a spin cycle of C ($C=2^n$,n=1,2,..15) the total count rate T, as well as a foreground rate F from selected bins are summed. When reaching $C=2^n$ the rate F is set into relation to T. If

$F \geq \frac{T}{H}$ with H=high flux ratio=8 (default)

then high flux is detected and a shorter integration time is chosen. If

$F \leq \frac{T}{L}$ with L=low flux ratio = 64 (default)

then low flux is detected and a larger integration time is chosen.

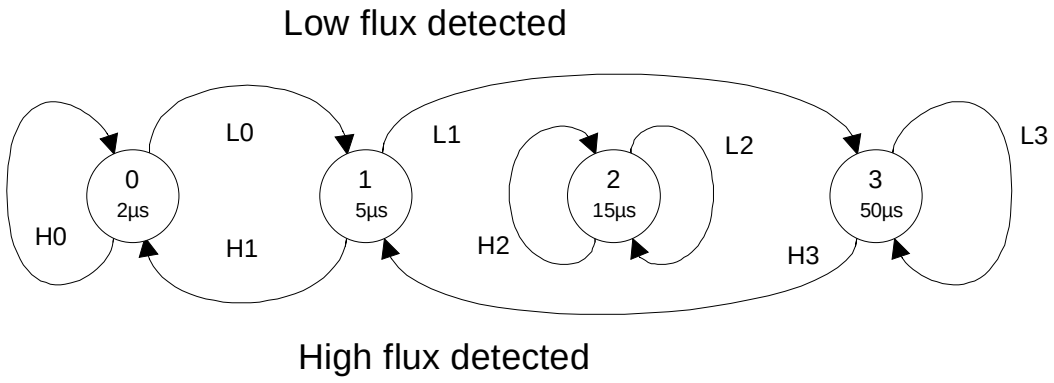

Fig. 2-1 Autoswitching transitions

The variables H and L can be any integer numbers in the range 1…255. The default spin cycle is C=32.

The default transitions between integration times initiated by autoswitching are displayed in Fig. 2-1. Please note that the 15 µs integration time is not used for the current autoswitching algorithm. Each transition can be reprogrammed.

For summation of F and T the algorithm allows the selection of

1. the IDs (default are ID 4, 5 and 6),

2. the bins to be examined (default are all 16 bins) and

3. the bins to be used for F (default bins are 6 to 15).

2.2 Parameter changes

Parameter changes are performed by standard program uploads. In the following Table 2-1 the respective addresses and the current default values are displayed. Changes can be stored in NVRAM by issuing the RAPID command *ZERCFGSS 0*. Reloading of the data set at a later time can be done through the command *ZERCFGSS 1*.

Address	Length	Default	Comment
OFFS + 24EECh	1 Word	001Fh	Spin cycle C-1=2^n-1
OFFS + 24EEEh	1 Word	0070h	ID mask (1: enabled), default ID 4,5 and 6
OFFS + 24EF0h	1 Word	FFFFh	Bin mask, all bins used for F and T calc.
OFFS + 24EF2h	1 Word	FFC0h	Bins 6 to 15 are used for F
OFFS + 24EF4h	1 Byte	8	High flux ratio H
OFFS + 24EF5h	1 Byte	64	Low flux ratio L
OFFS + 24EFEh	1 Byte	0	Target state for transition H0 (Source state 0)
OFFS + 24EFFh	1 Byte	0	Target state for transition H1 (Source state 1)
OFFS + 24F00h	1 Byte	2	Target state for transition H2 (Source state 2)
OFFS + 24F01h	1 Byte	1	Target state for transition H3 (Source state 3)
OFFS + 24F02h	1 Byte	1	Target state for transition L0 (Source state 0)
OFFS + 24F03h	1 Byte	3	Target state for transition L1 (Source state 1)
OFFS + 24F04h	1 Byte	2	Target state for transition L2 (Source state 2)
OFFS + 24F05h	1 Byte	3	Target state for transition L3 (Source state 3)

Table 2-1 User-definable parameters for autoswitching algorithm [i]

Remember, that variables of the type WORD have to be written in Intel format into memory, i.e. low byte first, then high byte.

3 IES science data formatting

3.1 Default formatting

For the IES data types E-3DD(NM), E-PAD and the IES section in the HK it is possible to redefine the bins, that are summed up. The data type E-3DD(BM) is not fitted with this possibility, because in conjunction with the HK data every possible bin is already covered.

Bin number Range: 0…15	E-3DD (BM) Range: 0…11	E-3DD (NM) Range: 0…7	E-PAD Range: 0…1	HK Range: 0…3
0				0
1				1
2	0			
3	1	0		
4	2	1		
5	3			
6	4	2	0	
7	5	3	0	
8	6	4	0	
9	7	5	0	
10	8	6	1	
11	9	6	1	
12	10	7	1	
13	11	7	1	
14				2
15				3

Table 3-1 Source bins for IES science data types

3.2 Parameter changes

The redefinition can be done easily by writing into dedicated memory locations. Parameter changes are performed by standard program uploads. In the following Table 2-1 the respective addresses and the current default values are displayed

Every of the 16 possible bins, that can be used for science data, is represented by a single bit in the word variables of the following Table 3-2. All bins with a ’1’ will be used for summing up, bins with cleared bits are not used.

Address	Length	Default	Comment
OFFS + 24F06h	1 Word	03C0h	E-PAD bin pattern, direction 1, interval 0
OFFS + 24F08h	1 Word	3C00h	E-PAD bin pattern, direction 1, interval 1

Address	Length	Default	Comment
OFFS + 24F0Ah	1 Word	03C0h	E-PAD bin pattern, direction 2, interval 0
OFFS + 24F0Ch	1 Word	3C00h	E-PAD bin pattern, direction 2, interval 1
OFFS + 24F0Eh	1 Word	03C0h	E-PAD bin pattern, direction 3, interval 0
OFFS + 24F10h	1 Word	3C00h	E-PAD bin pattern, direction 3, interval 1
OFFS + 24F12h	1 Word	0008h	E-3DD (NM), bin pattern for interval 0
OFFS + 24F14h	1 Word	0010h	E-3DD (NM), bin pattern for interval 1
OFFS + 24F16h	1 Word	0040h	E-3DD (NM), bin pattern for interval 2
OFFS + 24F18h	1 Word	0080h	E-3DD (NM), bin pattern for interval 3
OFFS + 24F1Ah	1 Word	0100h	E-3DD (NM), bin pattern for interval 4
OFFS + 24F1Ch	1 Word	0200h	E-3DD (NM), bin pattern for interval 5
OFFS + 24F1Eh	1 Word	0C00h	E-3DD (NM), bin pattern for interval 6
OFFS + 24F20h	1 Word	3000h	E-3DD (NM), bin pattern for interval 7
OFFS + 24F22h	1 Word	0001h	HK, bin pattern for channel 0
OFFS + 24F24h	1 Word	0002h	HK, bin pattern for channel 1
OFFS + 24F26h	1 Word	4000h	HK, bin pattern for channel 2
OFFS + 24F28h	1 Word	8000h	HK, bin pattern for channel 3

Table 3-2 User-definable parameters for science data formatting [i]

Remember, that variables of the type WORD have to be written in Intel format into memory, i.e. low byte first, then high byte. The changes can be stored in NVRAM by issuing the RAPID command *ZERCFGSS 0*. Reloading of the data set at a later time can be done through the command *ZERCFGSS 1*.

4 Command examples

The following examples of command sequences shall provide a guideline how to change the IES parameters. All commands and the CRC calculation are explained in the document „Instrument User's Guide", which is the Annex A1 of the „Flight Operation User Manual" for RAPID.

4.1 Example 1: Changing the two-parameter LUT description

In this section the command sequences are developed that are needed for changing the parameter P for ID2 (2µs integration time) in the current 2-parameter LUT description on the RAPID F1 (phoenix) unit. The default parameter is 1Bh (see Table 1-3) and the address is 25175h. This parameter shall be changed to 04h and the new definition stored into NVRAM.

1. Define the RAMCHECK address with the command BERRCADS. The two-parameter description starts at 25172h and ends in 251BDh. The CRC results to 4Ah from the bytes 02h, 51h, 72h, 02h, 51h and BDh. The complete command is 4806h, 8802h, 8851h, 8872h, 8802h, 8851h, 88BDh and C84Ah.

2. Switch on RAMCHECK mode by issuing command ZERIRCKS 01h.

3. Define the memory load address. The command BERPLADS is issued with the address 25175h. The CRC results to EDh from the bytes 02h, 51h and 75h. The complete command is: 4503h, 8502h, 8551h, 8575h, C5EDh.

4. Load up the single byte 04h with the command BERMLDCS. The CRC results as 84h from the byte 04h. The complete command is: 4401h, 8404h, C484h. The result of this commanding can be seen in the EDBs, that are already filled with RAMCHECK results.

5. Store the new description in NVRAM by issuing the command ZERCFGSS 0.

6. Switch off RAMCHECK mode by issuing command ZERIRCKS 00h.

7. Incorporate the changes in the description by sending the command ZERELUTS 40h. The parameter for this command could also be 00h, but 40h leads to autoswitching mode off. This provides time for also checking the 16-parameter description and the expanded LUT in the following.

8. Define the RAMCHECK address with the command BERRCADS. The 16-parameter description, that should have changed with the last command, ranges from 024F2Eh to 025171h. The CRC results as 0Ch from the bytes 02h, 4Fh, 2Eh, 02h, 51h and 71h. The complete command is 4806h, 8802h, 884Fh, 882Eh, 8802h, 8851h, 8871h and C80Ch.

9. Switch on RAMCHECK mode by issuing command ZERIRCKS 01h.

10. Check the new 16-parameter description and switch off RAMCHECK by issuing command ZERIRCKS 00h.

11. Define the RAMCHECK address with the command BERRCADS. The complete expanded LUT in RAM ranges from 013F44h to 014843h for the ID1 to 9. The address of the expanded version of the LUT for ID2 ranges from 014044h to 014143h. The CRC results as 0Bh from the bytes 01h, 40h, 44h, 01h, 41h and 43h. The complete command is 4806h, 8801h, 8840h, 8844h, 8801h, 8841h, 8843h and C80Bh.

12. Switch on RAMCHECK mode by issuing command ZERIRCKS 01h.

13. Check the new LUT and switch off RAMCHECK by issuing command ZERIRCKS 00h.

The above sequence of 13 steps is useful for thoroughly checking every (2-,16-parameter, expanded) LUT description. The minimum steps for changing, storing and incorporating a change in the 2-parameter description are the steps 3,4,5 and 7.

4.2 Example 2: Changing the bins used for F in autoswitching algorithm

In this section the bins used for the counter F of the autoswitching algorithm (compare section 2.1) on the RAPID F1 (phoenix) unit shall be changed from the default bins 6-15 to 7-14. Accordingly the bin mask has to be changed from FFC0h (compare Table 2-1) to 7F80h. This new mask shall be made permanent by storing into NVRAM.

1. Define the memory load address. The command BERPLADS is issued with the address 24EF2h. The CRC is results as F5h from the bytes 02h, 4Eh and F2h. The complete command is: 4503h, 8502h, 854Eh, 85F2h, C5F5h.

2. Load up 1 word (2 bytes) with the command BERMLDCS. The word variable 7F80h must be uploaded bytewise, low byte first. The CRC results as FAh from the bytes 80h and 7Fh. The complete command is: 4402h, 8480h, 847Fh and C4FAh.

3. Store the new description in NVRAM by issuing the command ZERCFGSS 0.

The reaction of the DPU on the above commands can be monitored by doing RAMCHECK on the address range 24EF2h to 24EF3h during or after upload.

4.3 Example 3: Adding the content of bin 2 to HK channel 1

In this example the HK channel 1 (compare Table 3-1) on the RAPID F1 (phoenix) unit shall be expanded from just containing the bin 1 count rates to containing the sum of bins 1 and 2. The respective bin pattern at location 24F24h (compare Table 3-2)will change from 0002h to 0003h. Since just the low byte is changed, only a single byte upload at address 24F24h is required.

1. Define the memory load address. The command BERPLADS is issued with the address 24F24h. The CRC is results as 5Fh from the bytes 02h, 4Fh and 24h. The complete command is: 4503h, 8502h, 854Fh, 8524h, C55Fh.

2. Load up 1 byte with the command BERMLDCS. The CRC results as 63h from the byte 03h. The complete command is: 4401h, 8403h and C463h.

3. Store the new description in NVRAM by issuing the command ZERCFGSS 0.

The reaction of the DPU on the above commands can be monitored by doing RAMCHECK on the address 24F24h during or after upload.

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[i] Value OFFS differs between RAPID-units: for RAPID F1 (phoenix) use OFFS=0000h,
for RAPID F6-F8 use OFFS=2408h.