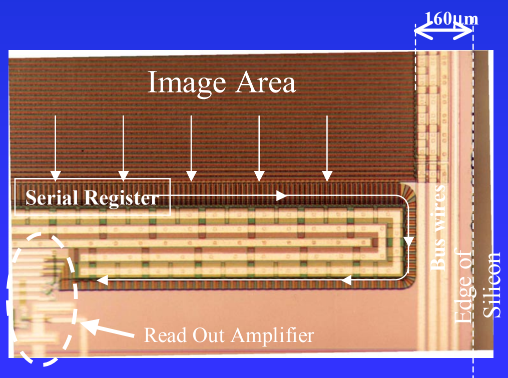
Space Instrumentation (10a)

Lectures for the IMPRS June 23 to June 27 at MPAe Lindau
Compiled/organized by Rainer Schwenn, MPAe,
supported by Drs. Curdt, Gandorfer, Hilchenbach, Hoekzema, Richter, Schühle

Thu, 26.6., 15:00 CCD and APS principles (Pardowitz)



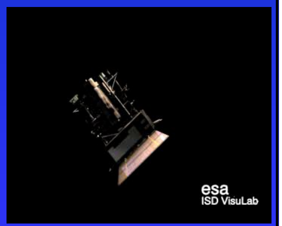
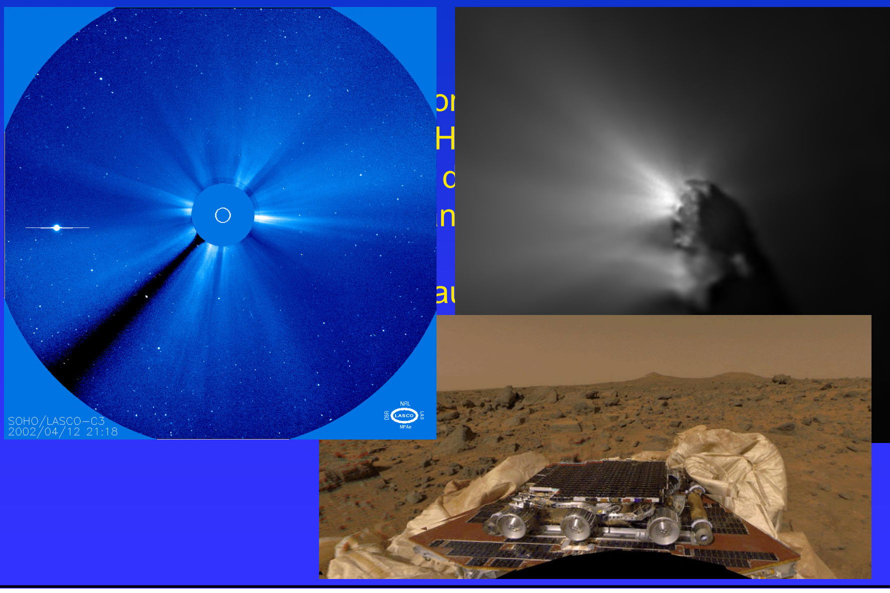


Image Detectors:
CCD and APS

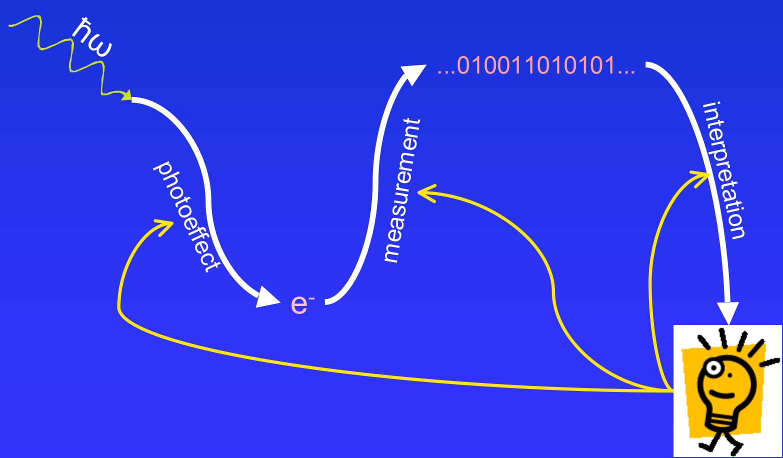
- Introduction
- CCD history
- CCD structure
- Charge generation and collection
- Charge transfer & readout
- APS principles
- Performance parameters of CCD‘s

I. Pardowitz IMPRS – 26.6.2003

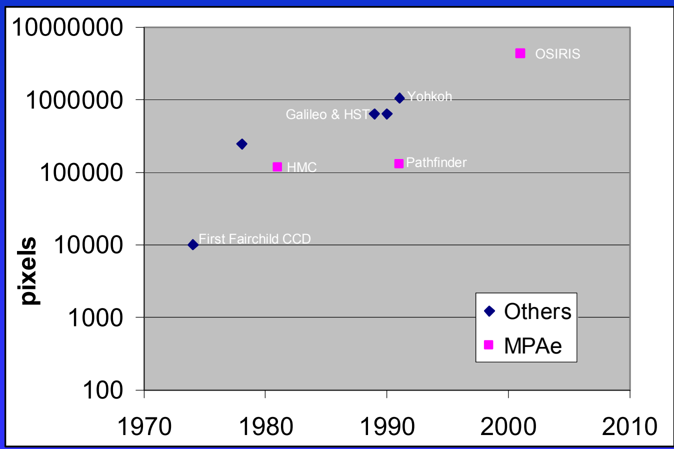
Images and reality



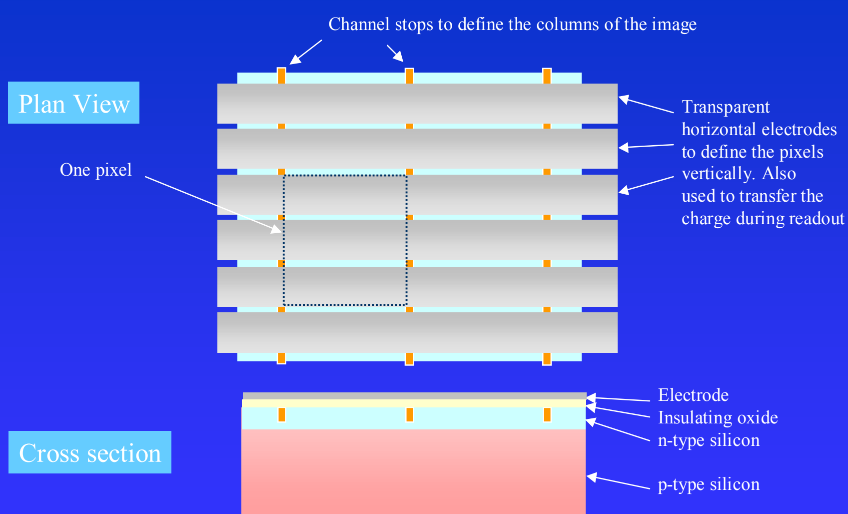
From photon to knowledge



Evolution of space CCD‘s



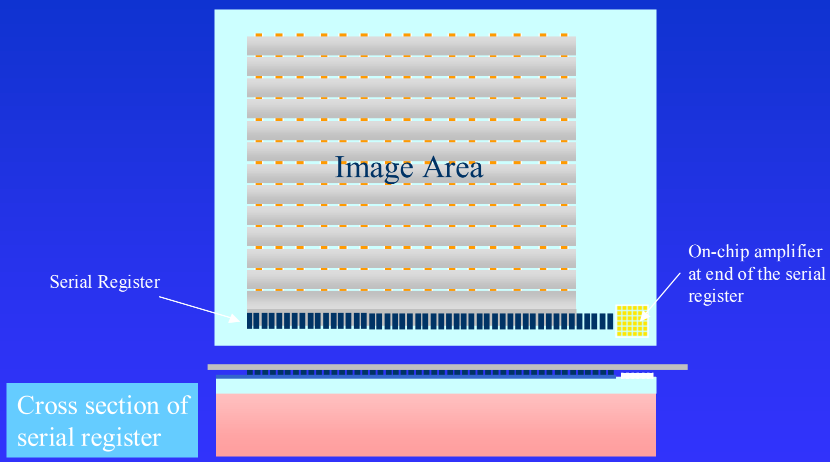
Structure of a CCD (1)



Every third electrode is connected together. Bus wires running down the edge of the chip make the connection. The channel stops are formed from high concentrations of Boron in the silicon.

Structure of a CCD (2)

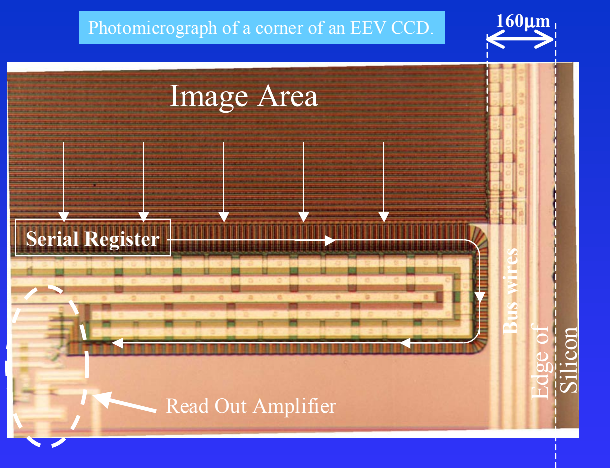
Below the image area (the area containing the horizontal electrodes) is the 'Serial register' . This also consists of a group of small surface electrodes. There are three electrodes for every column of the image area



Once again every third electrode is in the serial register connected together.

Structure of a CCD (3)

Photomicrograph of a corner of an EEV CCD.

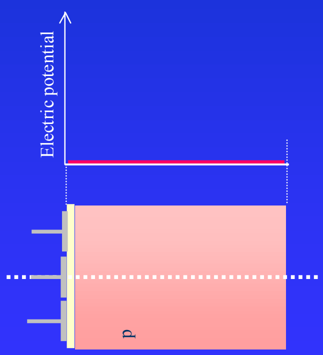


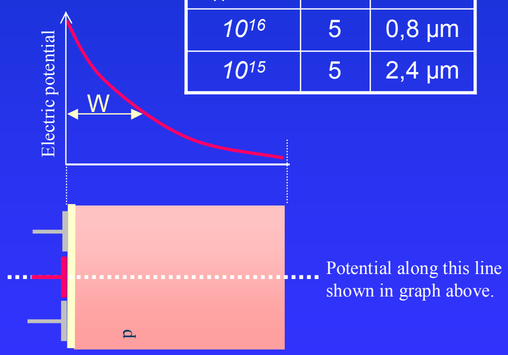
The serial register is bent double to move the output amplifier away from the edge of the chip. This useful if the CCD is to be used as part of a mosaic.The arrows indicate how charge is transferred through the device.

Electric Field in a CCD (1)

depletion width: $W(\Phi) \approx \sqrt{\dfrac{2\varepsilon\Phi}{qN_A}}$

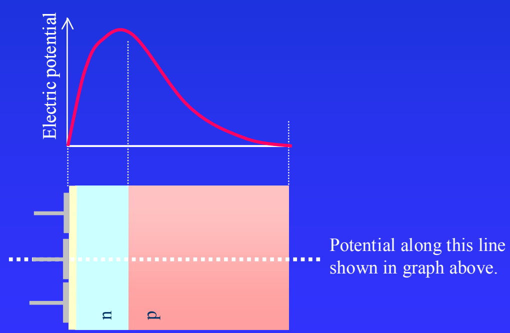
N_A [cm^{-3}]	Φ[V]	W
10^{16}	5	0,8 µm
10^{15}	5	2,4 µm





Electric Field in a CCD (2)

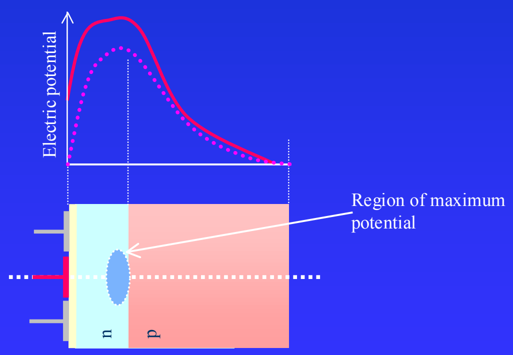
The n-type layer contains an excess of electrons that diffuse into the p-layer. The p-layer contains an excess of holes that diffuse into the n-layer. This structure is identical to that of a diode junction. The diffusion creates a charge imbalance and induces an internal electric field. The electric potential reaches a maximum just inside the n-layer, and it is here that any photo-generated electrons will collect. All science CCDs have this junction structure, known as a **'Buried Channel'**. It has the advantage of keeping the photo-electrons confined away from the surface of the CCD where they could become trapped. It also reduces the amount of thermally generated noise (dark current).



Cross section through the thickness of the CCD

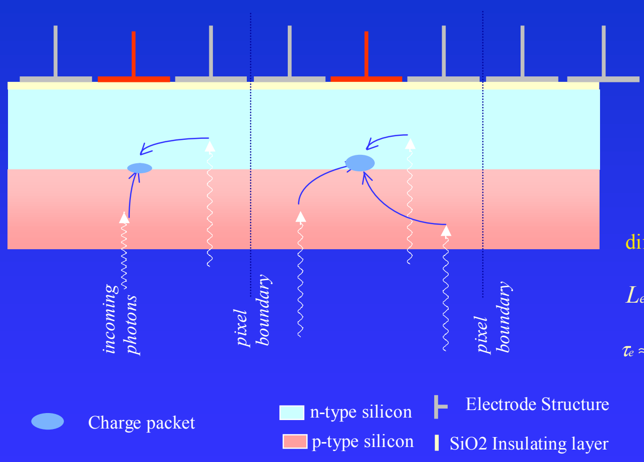
Electric Field in a CCD (3)

During integration of the image, one of the electrodes in each pixel is held at a positive potential. This further increases the potential in the silicon below that electrode and it is here that the photoelectrons are accumulated. The neighboring electrodes, with their lower potentials, act as potential barriers that define the vertical boundaries of the pixel. The horizontal boundaries are defined by the channel stops.



Charge Collection in a CCD (1)

Photons entering the CCD create electron-hole pairs. The electrons are then attracted towards the most positive potential in the device where they create ‘charge packets’. Each packet corresponds to one pixel



diffusion length:

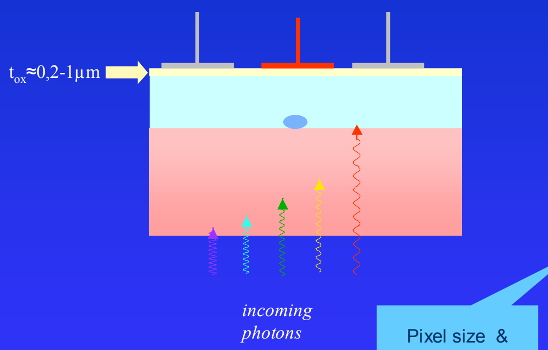
$$L_e = \sqrt{\frac{kT}{e}\mu_e \tau_e}$$

$\tau_e \approx 1\mu s$; $L_e \approx 50\mu m$

Charge Collection in a CCD (2)

Spectral sensitivity

a.) Absorption depth in Si



blue	450 nm	0,4 µm
green	550 nm	1,5 µm
red	640 nm	3,0 µm
IR	800 nm	10,5 µm

b.) Charge capacity per unit area

$$\frac{1}{C} = \frac{t_{ox}}{\varepsilon_{ox}} + \frac{W(\Phi)}{\varepsilon_{Si}}$$

$C \approx 10^{12}$ e^-/cm^2

Pixel size & Dynamic Range

Blooming

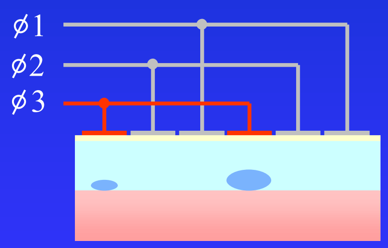
typ. pixel size= $(10\mu m)^2$

charge capacity = 50-200 10^3 e^-/pixel

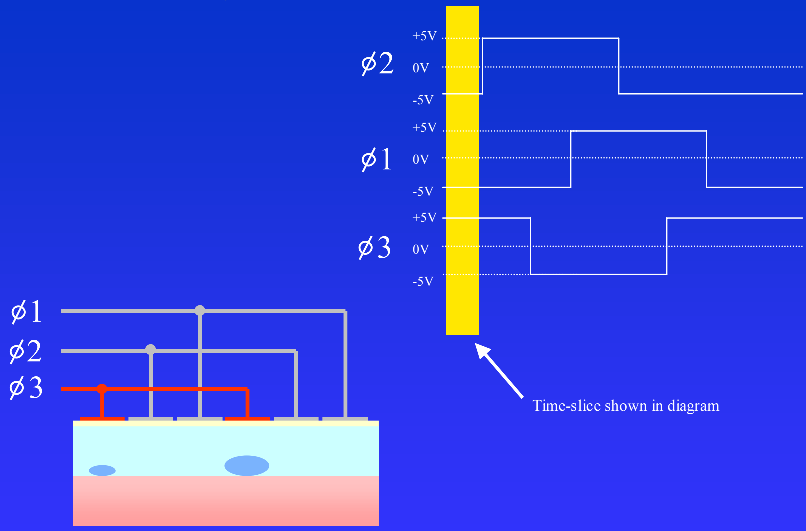
Charge Transfer in a CCD (1)

In the following few slides, the implementation of the 'conveyor belts' as actual electronic structures is explained.

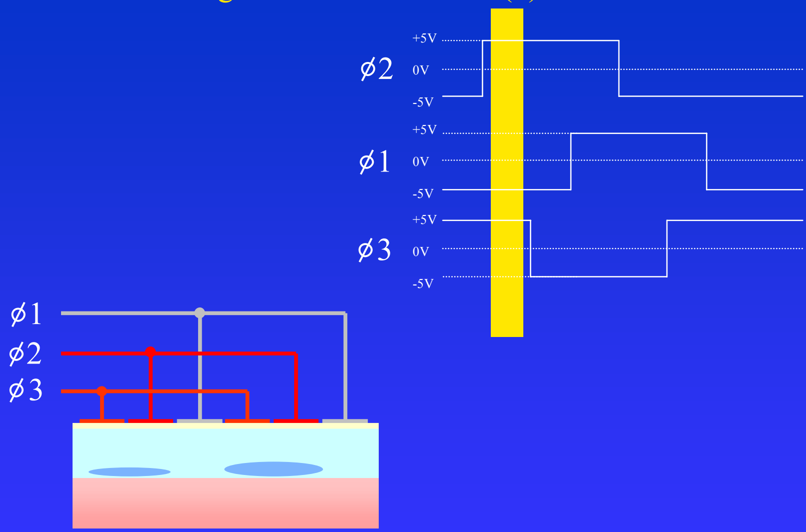
The charge is moved along these conveyor belts by modulating the voltages on the electrodes positioned on the surface of the CCD. In the following illustrations, electrodes colour coded red are held at a positive potential, those coloured grey are held at a negative potential.

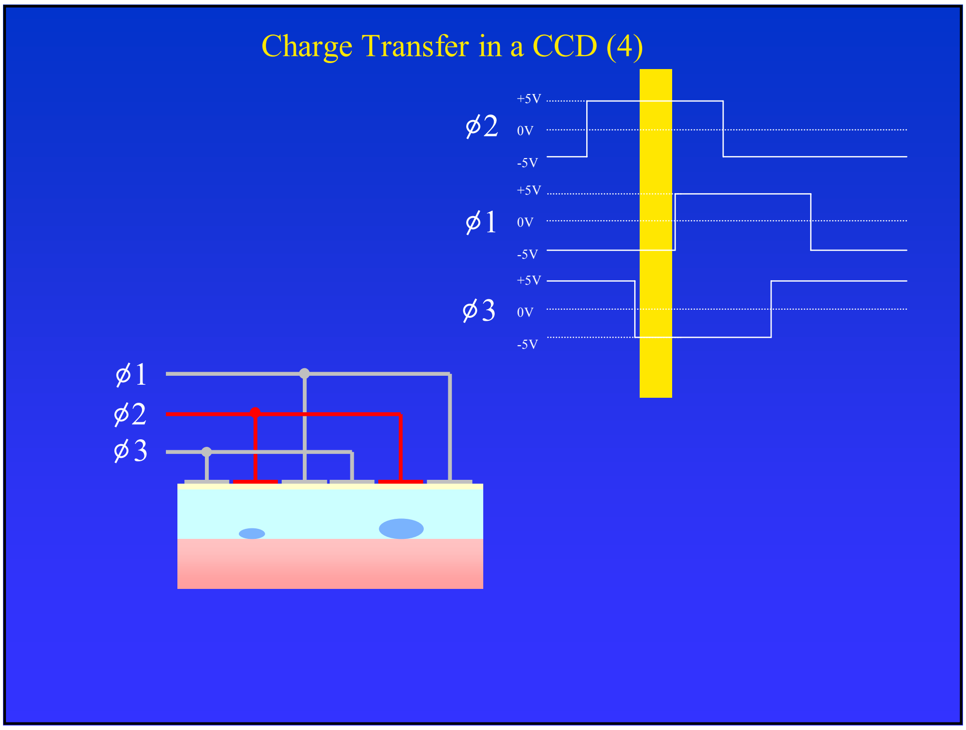


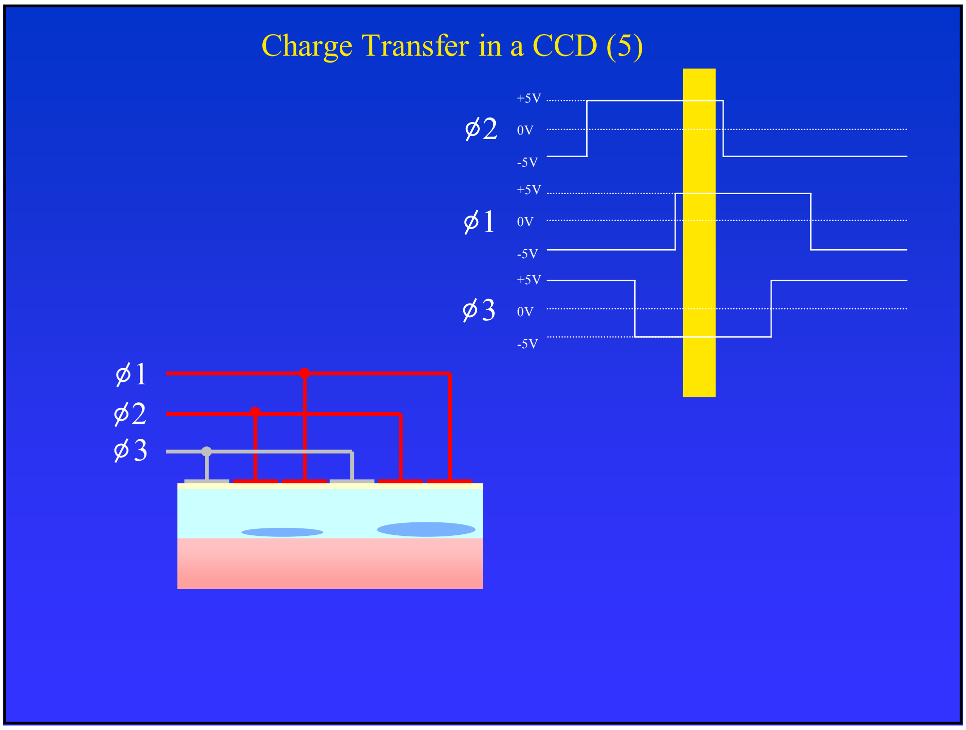
Charge Transfer in a CCD (2)

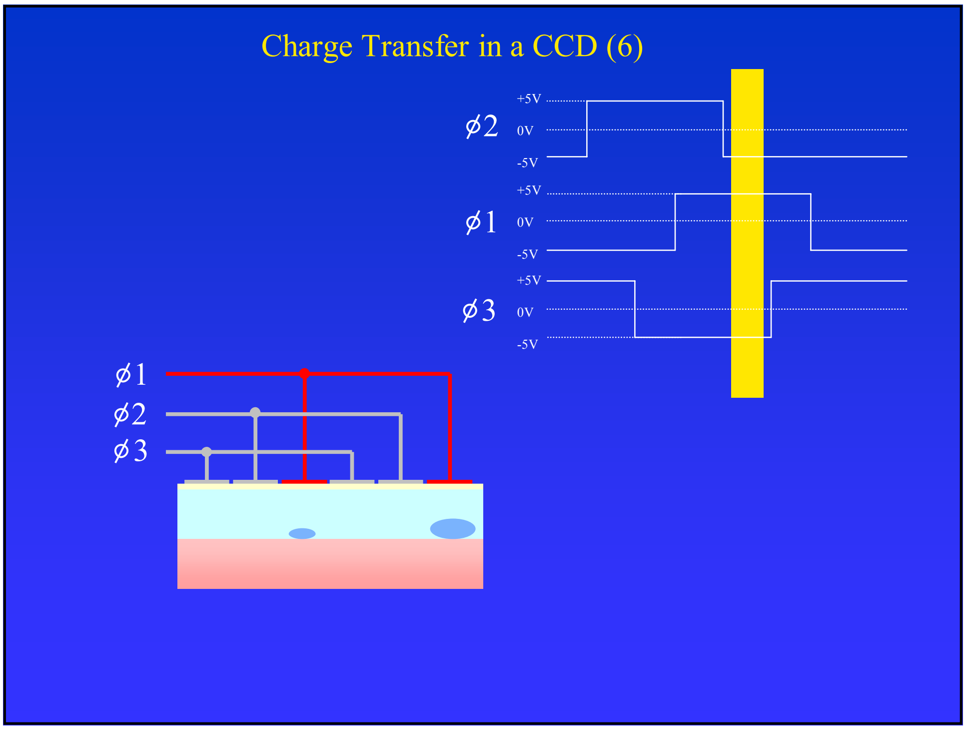


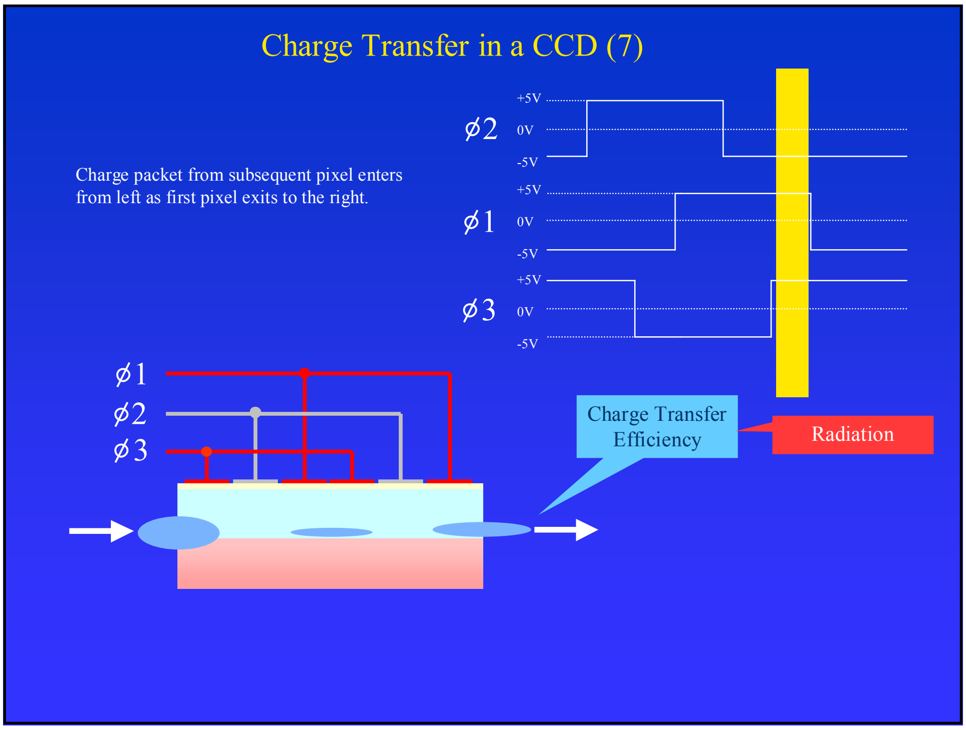
Charge Transfer in a CCD (3)

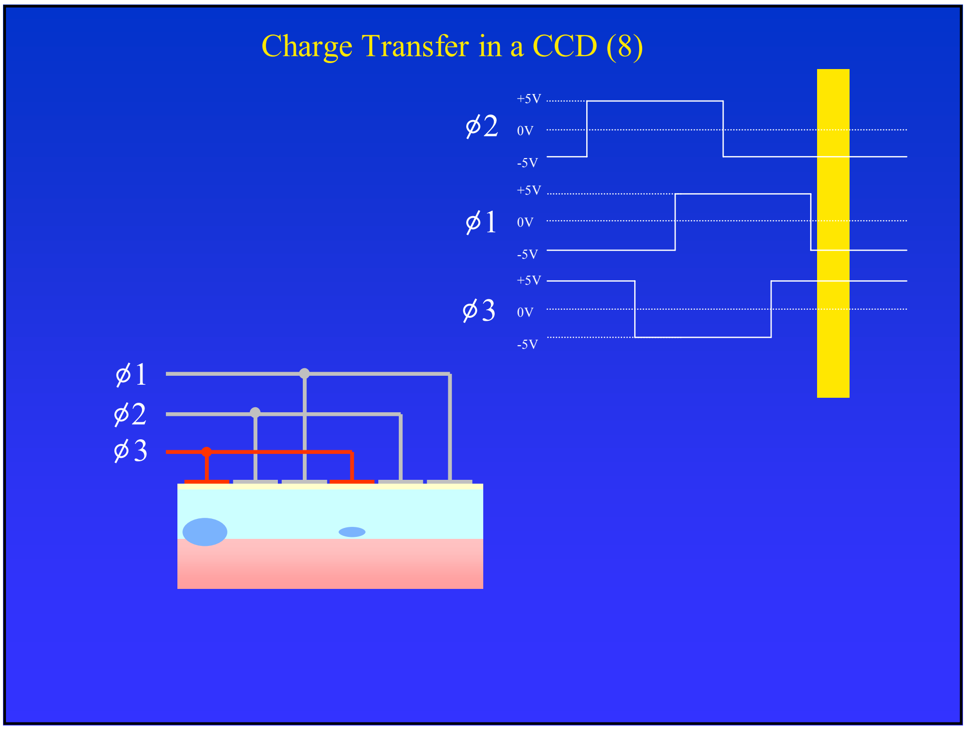


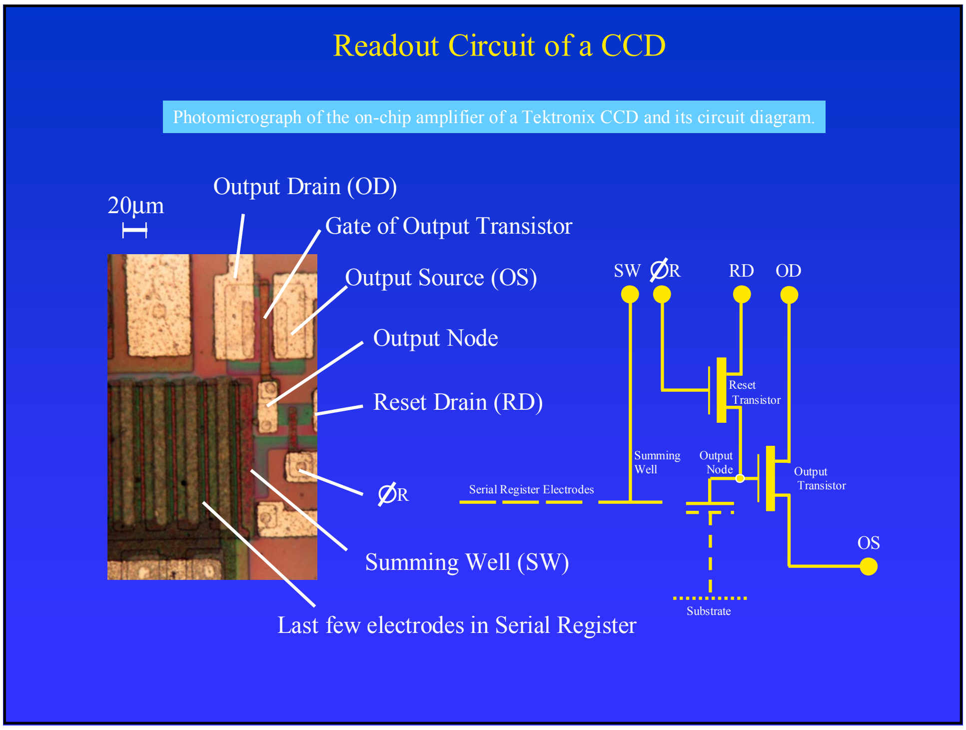

Charge Transfer in a CCD (4)
ϕ2
ϕ1
ϕ3
+5V
0V
-5V
ϕ1
ϕ2
ϕ3


Charge Transfer in a CCD (5)
ϕ2
ϕ1
ϕ3
+5V
0V
-5V
ϕ1
ϕ2
ϕ3


Charge Transfer in a CCD (6)
ϕ2
ϕ1
ϕ3
+5V
0V
-5V
ϕ1
ϕ2
ϕ3


Charge Transfer in a CCD (7)
Charge packet from subsequent pixel enters from left as first pixel exits to the right.
ϕ2
ϕ1
ϕ3
+5V
0V
-5V
ϕ1
ϕ2
ϕ3
Charge Transfer Efficiency
Radiation

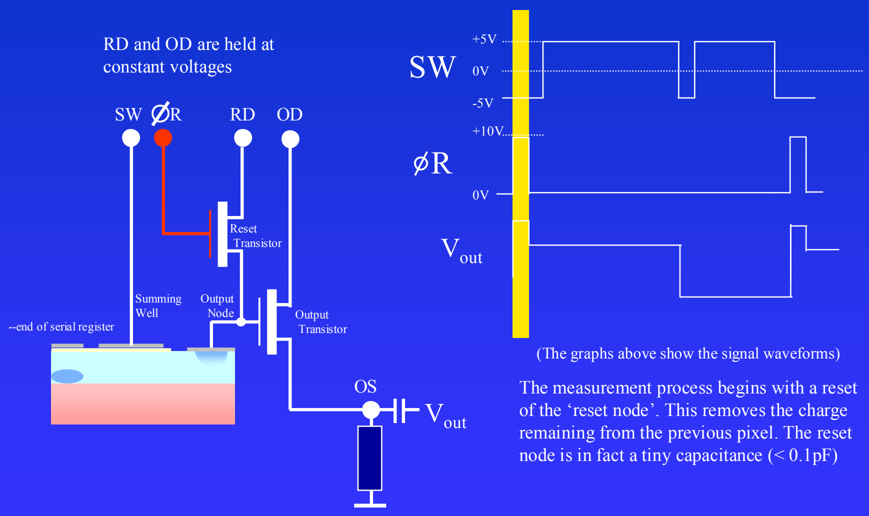

Charge Transfer in a CCD (8)
+5V
ϕ2
0V
-5V
+5V
ϕ1
0V
-5V
+5V
ϕ3
0V
-5V
ϕ1
ϕ2
ϕ3


Readout Circuit of a CCD
Photomicrograph of the on-chip amplifier of a Tektronix CCD and its circuit diagram.
20μm
Output Drain (OD)
Gate of Output Transistor
Output Source (OS)
Output Node
Reset Drain (RD)
ØR
Summing Well (SW)
Last few electrodes in Serial Register
SW
ØR
RD
OD
Reset Transistor
Summing Well
Output Node
Output Transistor
Serial Register Electrodes
OS
Substrate

On-Chip Amplifier (1)

The on-chip amplifier measures each charge packet as it pops out the end of the serial register.

RD and OD are held at constant voltages

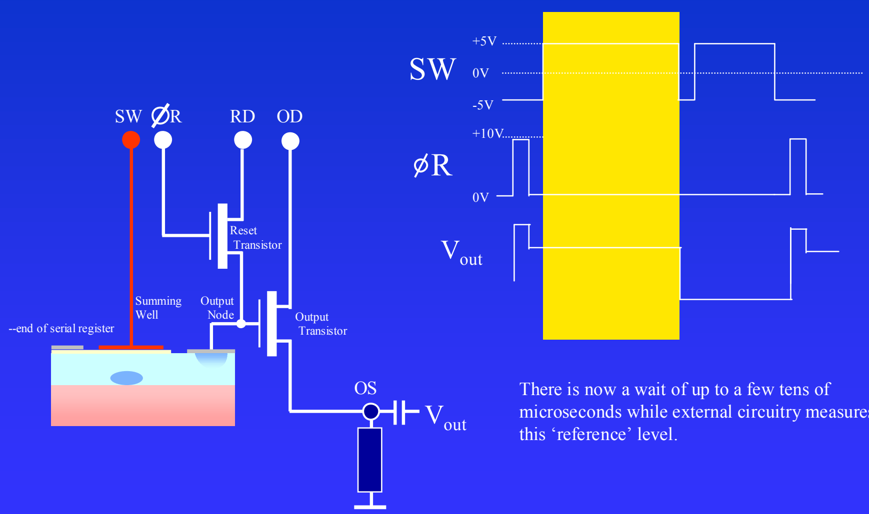


(The graphs above show the signal waveforms)

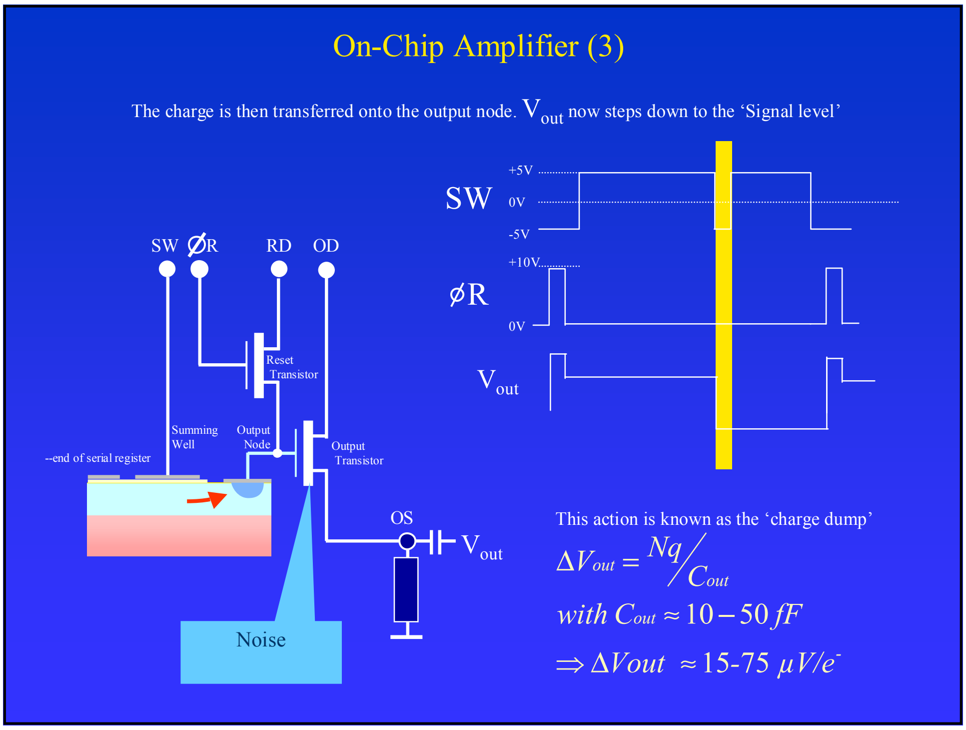
The measurement process begins with a reset of the 'reset node'. This removes the charge remaining from the previous pixel. The reset node is in fact a tiny capacitance (< 0.1pF)

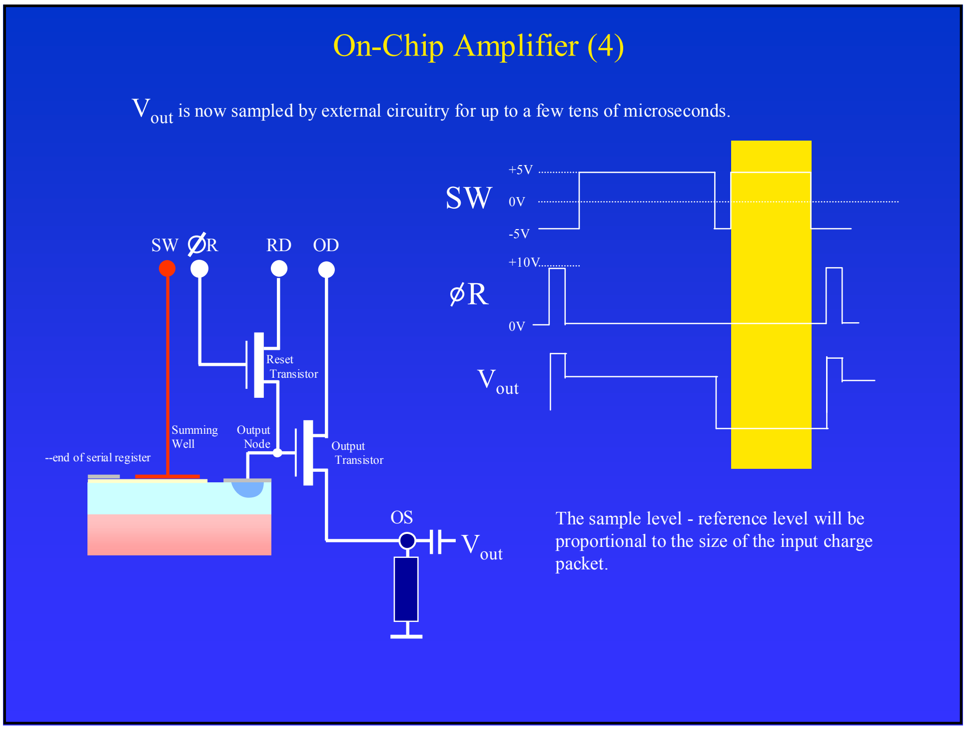
On-Chip Amplifier (2)

The charge is then transferred onto the Summing Well. V_{out} is now at the 'Reference level'



There is now a wait of up to a few tens of microseconds while external circuitry measures this 'reference' level.

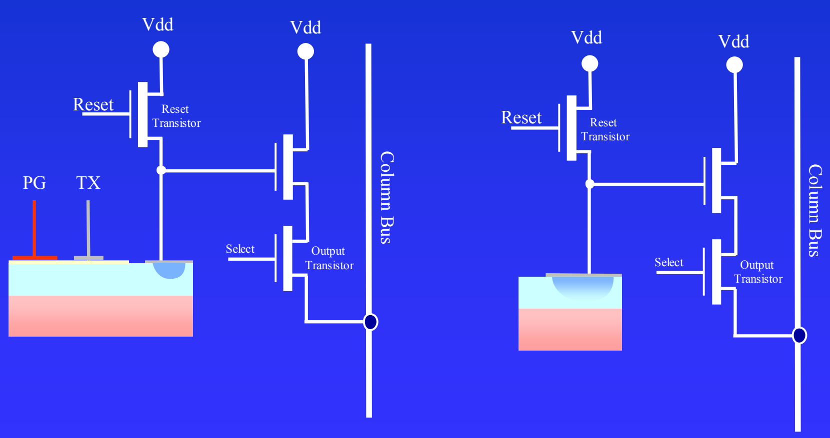

On-Chip Amplifier (3)
The charge is then transferred onto the output node. V_{out} now steps down to the 'Signal level'
SW
+5V
0V
-5V
øR
+10V
0V
V_{out}
SW ØR RD OD
Reset Transistor
Summing Well
Output Node
Output Transistor
--end of serial register
OS
V_{out}
Noise
This action is known as the 'charge dump'
$\Delta V_{out} = Nq / C_{out}$
with $C_{out} \approx 10-50\,fF$
$\Rightarrow \Delta V_{out} \approx$ 15-75 $\mu V/e^-$


On-Chip Amplifier (4)
V_{out} is now sampled by external circuitry for up to a few tens of microseconds.
SW
+5V
0V
-5V
øR
+10V
0V
V_{out}
SW ØR RD OD
Reset Transistor
Summing Well
Output Node
Output Transistor
--end of serial register
OS
V_{out}
The sample level - reference level will be proportional to the size of the input charge packet.

Active Pixel Sensors (1)

with photogate

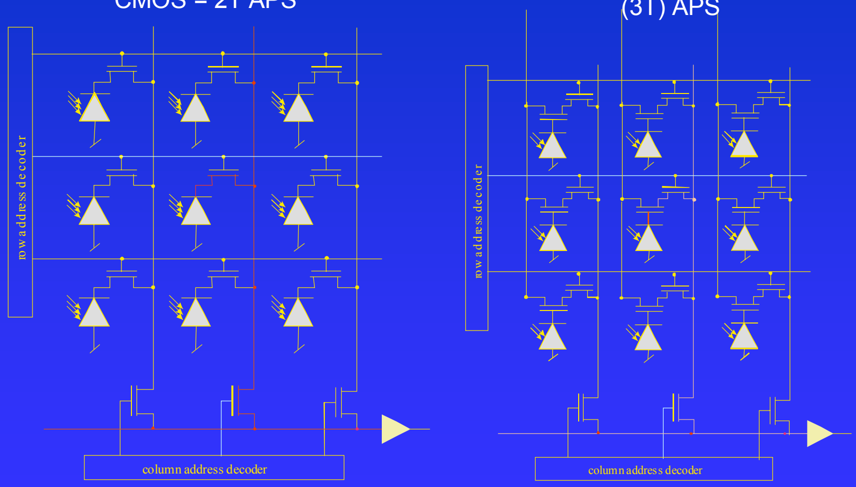
with photodiode



APS readout

CMOS = 2T APS

(3T) APS



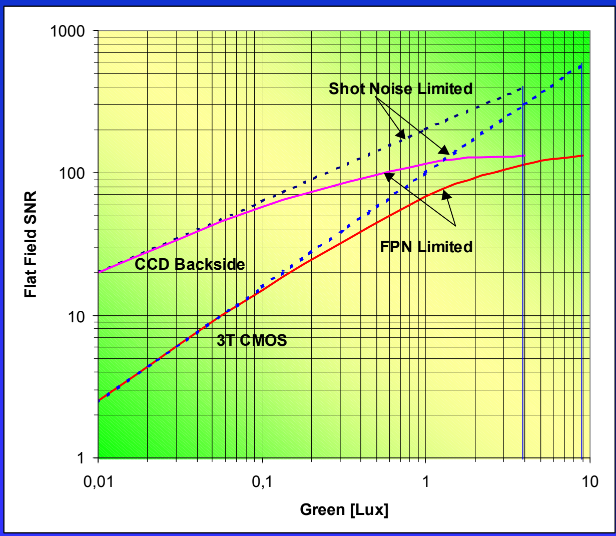
Performance Parameters(1)

- Spectral range
- QE = quantum efficiency
- Noise
- Dynamic range
- CCE = Charge Collection Efficiency
- Dark current
- CTE = Charge Transfer Efficiency

Performance Parameters (2)

- Number of pixels
- Framerate
- Radiation hardness
- Power requirements
- Chip count
- Technology / Market / Price

Signal-to-Noise



Quelle:
James Janesick. 2002

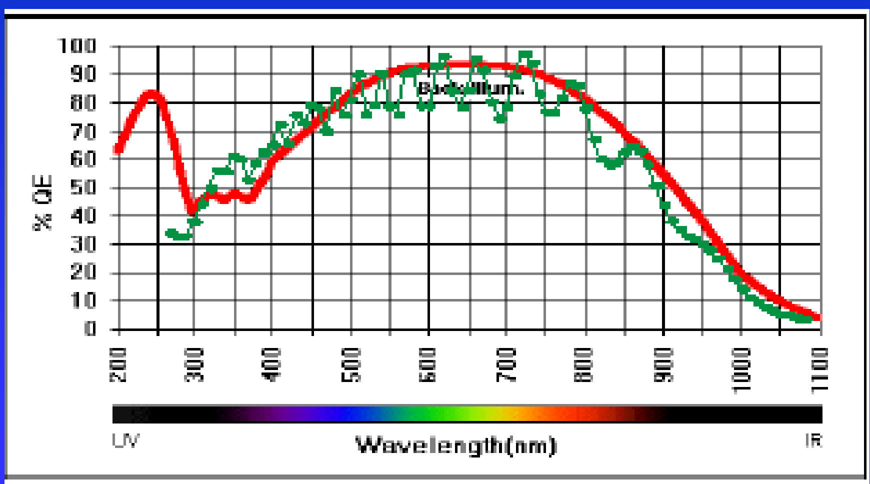
Photodetector materials

Material	E_{gap}(eV)	λ [nm]	band
Si	1,12	1100	Visible
GaAs	1,42	875	Visible
Ge	0,66	1800	NIR
InGaAs	0,73-0,47	1700-2600	NIR
InAs	0,36	3400	NIR
InSn	0,17	5700	IR
HgCd	0,7-0,1	1700-12500	NIR-FIR

Other detectors

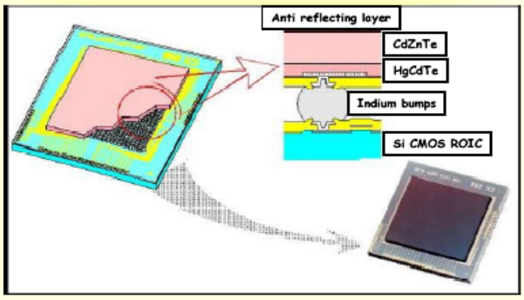
- PtSi (3-5 um)
- HgCdTe (3-5 or 8-10 um)
- CdZnTe
- QWIP (8-10 um)
- AlGaN (300 nm)

QE = quantum efficiency



Cooled IR Detector Technology

Semiconductor: HgCdTe | **Photovoltaic Detectors**



Hybrid Sensor Architecture